Q.P. Code:19EC4210 **R19**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

M.Tech I Year II Semester Regular Examinations October-2020

Low Power VLSI Design

(VLSI)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	What are the Bi-CMOS manufacturing and Integration considerations.	**6M**
	b	Demonstrate the advantages in the production of Graded-Drain structures.	**6M**
		OR	
2	**a**	Explain about the Junction isolation in the SBC process.	**6M**
	b	Explain the operation of Oxide-isolated Bipolar transistors.	**6M**

UNIT-II

3	**a**	Develop the steps in implementing copper metallization in deep sub micron process? Explain.	**6M**
	b	Explain BSIM2 and BSIM3 spice models.	**6M**
		OR	
4	**a**	Explain Lateral BJT on SOI.	**6M**
	b	What are the limitations of the MOSFET characteristics?	**6M**

UNIT-III

5	**a**	Draw the circuit for Full Swing complimentary MOS circuit for two input NAND gate and explain its operation.	**6M**
	b	Draw the circuit for High performance complimentary coupled Bi-CMOS three input NAND gate and explain its working.	**6M**
		OR	
6	**a**	Examine Full swing Bi-CMOS Digital circuits employing schottky diodes.	**6M**
	b	Explain FS-Multi drain Complementary Bi-CMOS Buffers with neat diagram.	**6M**

UNIT-IV

7	**a**	Explain the need for Low-power latches and flip-flops.	**6M**
	b	Write short notes on the evolution of latches and flip-flops.	**6M**
		OR	
8	**a**	Explain double-edge triggered flip-flops with neat sketch.	**6M**
	b	Examine different power dissipation measures in detail.	**6M**

UNIT-V

9	**a**	Examine different low power techniques for SRAM.	**6M**
	b	What is SRAM? Draw the circuit of SRAM.	**6M**
		OR	
10		Analyze various delay balancing techniques with a neat sketch.	**12M**

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